25 Spring ECEN 720: High-Speed Links: Circuits and Systems Pre-lab Report

Lab5: Equalization Circuits

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1. Design a passive CTLE as shown in Figure 7(a) to realize the transfer function as shown

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1. 3. Design a 4-bit parallel PRBS generator with 27-1 sequence length and an error detector circuit with a testing circuit at 2Gb/s with ideal blocks. Using the test circuit, you should be able to inject error data pattern and observe the error signal. An example is shown in Figure 13. Please show the simulation results. You may refer to the Appendix by Younghoon Song on how to build a parallel PRBS generator and detector.

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